AMENDMENTS TO THE CLAIMS:

1. (Currently Amended) A frequency divider comprising:

a first flip-flop without stacked transistors having a first clock input for receiving a clock

signal, the first flip-flop further comprising a first set input and a first non-inverted output; and

a second flip-flop without stacked transistors having a second clock input for receiving

a second clock signal that is substantially in anti-phase with the clock signal inputted into the

first clock input, a second set input coupled to the first non-inverted output, a second non-

inverted output and a second inverted output, wherein the second inverted output of the second

flip-flop being is coupled to the first set input of the first flip-flop for providing an inverted

output signal from said non-inverted output of the second flip-flop as feedback to the set input

of the first flip-flop; and

wherein said frequency divider does not have an additional controlled inverter for

providing a time delay.

2. (Currently Amended) A frequency divider as claimed in claim 1, wherein a period of

the second clock signal is of the same order of magnitude as a delay through the second inverted

output an inverter stage of the divider.

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3. (Currently Amended) A frequency divider as claimed in claim 1, wherein a controllable

switch is coupled to said first set input of the first slip-flop flip-flop and to the second inverted

output of the second flip-flop and further comprises a third output Qa2 coupled to said

controllable switch, wherein said controllable switch being controlled by the clock signal driving

the first flip-flop.

4. (Currently Amended) A frequency divider as claimed in claim 1, wherein a controllable

switch is coupled to the second inverted output of the second flip-flop further comprises a third

output, and wherein a controllable switch is coupled to a third output via resistive means.